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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHOWDHURY, AFROZA Y	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
01/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/511,447	TAKAHARA ET AL.	
	Examiner	Art Unit	
	Afroza Y. Chowdhury	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *8 and 11-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-10, and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/12/2007, 9/18/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 8 and 11-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected **Groups II and III**, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on **November 30, 2007**.

2. Applicant's election without traverse of **Groups I** in the reply filed on **November 30, 2007** is acknowledged.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "**gate driver circuit turns on and off the first switching elements two or more times during one frame period**" in claims 1, 4, and 5, "**image signal applied to each pixel is retained only once during the one frame period**" in claims 1, 2, 5, and 11, and "**gate driver circuit keeps the first switching elements off two horizontal scanning periods during one frame period**" in claim 11 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a) because they fail to show "**how many horizontal scanning period in each frame**" in **fig. 67** and **fig. 178** as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Regarding claims 1, 2, and 5, "**an image signal applied to each pixel is retained only once during the one frame period**" is not described in the specification.

Regarding claim 3, specification does not support "**the first current is larger than the second current**".

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamazaki et al.** (US Patent 6,765,549).

As to claim 3, Yamazaki et al. discloses a drive method for an EL display panel, the EL display panel comprising:

EL elements (fig. 3(111)) arranged in a matrix (fig. 2(101, 104));

driver transistors (fig. 3(109)) which supply current to be passed through the EL elements (fig. 3(111));

first switching elements (fig. 3(105)) placed in current paths of the EL elements (fig. 3(111)); and

a gate driver circuit (fig. 1(103)) which turns on and off the first switching elements (fig. 3(105)) for control (col. 8, line 67 – col. 9, line 9); and

a source driver circuit (fig. 1(102)) which supplies programming current to the driver transistors (col. 8, line 67 – col. 9, line 9), wherein:

a period during which a pixel row is selected and programmed with current is constructed from a first period and second period (col. 10, line 56 – col. 11, line 9)

a first current is applied during the first period (col. 11, line 64 – col. 12, line 3),

a second current is applied during the second period (col. 11, line 64 – col. 12, line 3).

Yamazaki et al. does not teach whether the first current is larger than the second current and the source driver circuit outputs the first current during the first period and outputs the second current during the second period which comes after the first period.

However, it is a design choice to make the driver circuit where the first current is larger than the second current and the source driver circuit outputs the first current during the first period and outputs the second current during the second period which comes after the first period.

8. Claims 1-2, 4-7, 9-10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamazaki et al.** (US Patent 6,765,549) in view of **Sekiya et al.** (US Patent 6,583,775).

As to claim 1, Yamazaki et al. discloses a drive method for an EL display panel, the EL display panel comprising:

EL elements (fig. 3(111)) arranged in a matrix (fig. 2(101, 104));

driver transistors (fig. 3(109)) which supply current to be passed through the EL elements (fig. 3(111));

first switching elements (fig. 3(105)) placed in current paths of the EL elements (fig. 3(111)); and

a gate driver circuit (fig. 1(103)) which turns on and off the first switching elements (fig. 3(105)) for control (col. 8, line 67 – col. 9, line 9);

wherein the gate driver circuit (fig. 1(103)) turns on and off the first switching elements two or more times during one frame period (fig. 5, col. 10, lines 25-33).

Yamazaki et al. does not explicitly teach an EL display panel where an image signal applied to each pixel is retained only once during the one frame period.

Sekiya et al. teaches an EL display panel where an image signal applied to each pixel is retained only once during the one frame period (col. 16, line 66 – col. 17, line 28).

Therefore, it is obvious to one skill in the art at the time of the invention was made to combine the image display panel apparatus of Sekiya et al. with the EL display device of Yamazaki et al. to make an EL display panel with improved picture quality.

As to claim 2, Yamazaki et al. teaches a drive method for an EL display panel, the EL display panel comprising:

EL elements (fig. 3(111)) arranged in a matrix (fig. 2(101, 104));

driver transistors (fig. 3(109)) which supply current to be passed through the EL elements (fig. 3(111));

first switching elements (fig. 3(105)) placed in current paths of the EL elements (fig. 3(111)); and

a gate driver circuit (fig. 1(103)) which turns on and off the first switching elements (fig. 3(105)) for control (col. 8, line 67 – col. 9, line 9).

Yamazaki et al. does not specifically teach an EL display panel where the gate driver circuit keeps the first switching elements off two horizontal scanning periods during one frame period, and an image signal applied to each pixel is retained only once during the one frame period.

Sekiya et al. teaches an EL display panel where the gate driver circuit keeps the first switching elements off two horizontal scanning periods during one frame period (fig. 15), and

an image signal applied to each pixel is retained only once during the one frame period (col. 16, line 66 – col. 17, line 28).

Therefore, it is obvious to one skill in the art at the time of the invention was made to combine the image display panel apparatus of Sekiya et al. with the EL display device of Yamazaki et al. to make an EL display panel in order to improve quality of moving pictures.

As to claim 4, Yamazaki et al. teaches a drive method for the EL display panel wherein the first switching elements (fig. 3(105)) are turned off periodically during one frame period (fig. 5).

As to claim 5, Yamazaki et al. teaches an EL display panel, comprising:

a source driver circuit (fig. 1(102)) which outputs an image signal (col. 8, lines 44-50);

EL elements (fig. 3(111)) arranged in a matrix (fig. 2(101, 104));

driver transistors (fig. 3(109)) which supply current to be passed through the EL elements (fig. 3(111));

first switching elements (fig. 3(105)) placed in current paths of the EL elements (fig. 3(111));

a first gate driver circuit (fig. 1(103)) which turns on and off the first switching elements (fig. 1(103)) for control (col. 8, line 67 – col. 9, line 9); and

a second gate driver circuit which turns on and off the second switching elements for control (col. 7, line 64); wherein:

the first gate driver circuit (fig. 1(103)) turns off the first switching elements a number of times during one frame period (fig. 5, col. 10, lines 25-33).

Yamazaki et al. does not specifically teach second switching elements that constitute paths used to transmit the image signal to the driver transistors.

However, it is obvious for an EL display to have second switching elements which constitute paths used to transmit the image signal to the driver transistors when a second gate driver is used.

Yamazaki et al. also does not explicitly teach an EL display panel where an image signal applied to each pixel is retained only once during the one frame period.

Sekiya et al. teaches an EL display panel where an image signal applied to each pixel is retained only once during the one frame period (col. 16, line 66 – col. 17, line 28).

Therefore, it is obvious to one skill in the art at the time of the invention was made to combine the image display panel apparatus of Sekiya et al. with the EL display

device of Yamazaki et al. to make an EL display panel with improved images and increased brightness.

As to claim 6, Yamazaki et al. teaches an EL display panel where the first and second gate driver circuits are formed in a same process as the driver transistors and the source driver circuit is made of a semiconductor chip (col. 8, lines 44-50).

As to claim 7, Yamazaki et al. discloses an EL display panel, comprising:

gate signal lines (fig. 3(106));

source signal lines (fig. 3(107));

a source driver circuit (fig. 3(102)) which outputs an image signal (col. 8, lines 44-50);

a gate driver circuit (fig. 3(103));

EL elements (fig. 3(111)) arranged in a matrix (fig. 2(101, 104));

driver transistors (fig. 3(109)) which supply current to be passed through the EL elements (fig. 3(111)); wherein:

the gate signal lines (fig. 3(106)) are connected to the gate driver circuit (figs. 1, 3(103)),

gate terminals of the second transistors are connected to the gate signal lines (col. 7, line 64), and

the gate driver circuit selects a plurality of gate signal lines and supplies the image signal to the driver transistors of a plurality of pixel rows (fig. 1, (col. 10, line 57 – col. 11, line 15).

Yamazaki et al. does not specifically teach an EL display panel comprising second transistors that constitute paths used to transmit an image signal to the driver transistors and source terminals of the second transistors are connected to the source signal lines.

Sekiya et al. teaches an image display apparatus where second transistors (fig. 5(TFT1)) constitute paths used to transmit an image signal to the driver transistors and source terminals of the second transistors are connected to the source signal lines (figs. 2, 5).

Therefore, it is obvious to one skill in the art at the time of the invention was made to combine the image display panel apparatus of Sekiya et al. with the EL display device of Yamazaki et al. to make an EL display panel with gate driver circuits.

As to claim 9, Yamazaki et al. teaches an EL display panel wherein the gate driver circuit selects a plurality of pixel rows at a time and applies the image signal from the source driver circuit to the plurality of pixel rows (col. 10, line 57 – col. 11, line 15).

As to claim 10, Yamazaki et al. teaches an EL display panel wherein the gate driver circuit is constructed of p-channel transistors (col. 16, lines 6-8, lines 32-42).

As to claim 15, Yamazaki et al. teaches an EL display apparatus comprising: the EL display panel and a receiver (fig. 17).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Afroza Y. Chowdhury whose telephone number is 571-270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
12/18/2007

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER